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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,136	02/26/2004	Naoki Ito	01-560	3489

23400 7590 12/19/2007

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EXAMINER	
JANAKIRAMAN, NITHYA	
ART UNIT	**PAPER NUMBER**
2123	

MAIL DATE	DELIVERY MODE
12/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/786,136	ITO ET AL.	
	Examiner	Art Unit	
	Nithya Janakiraman	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to the submission filed on 10/22/2007. Claims 1-16 are presented for examination.

Priority

1. Receipt is acknowledged of the certified copy of the foreign priority applications submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Response to Arguments- 35 U.S.C §102

2. Applicant's arguments filed 10/22/2007 have been fully considered but they are not persuasive.

3. Applicant argues on page 11, lines 1-3, that although Iino discloses different reset signals, Iino fails to teach or suggest outputting different vector addresses to change programs to be executed by the CPU. However, as is well-known in the art, the very function of reset signals is to cause different addresses to be loaded. In addition, as shown in column 11, lines 43-47, "After reset processing, the CPU core section **12** receives the activation enable signal **112** to start operation, and executes processing from a reset vector which is a start address of a program to be loaded immediately after reset." Thus, an address of a program is loaded subsequent to the reset process. Rejection maintained.

4. Applicant also argues on page 11, lines 8-9, that the vector address which is output, instead of the vector address corresponding to the reset vector address is a 'prescribed vector address' corresponding to the second signal. Again, as illustrated above, the purpose of a reset

signal is to cause different addresses to be loaded to change different programs. Thus, as Iino teaches a first and second reset signal, Iino teaches outputting corresponding first and second vector addresses. Column 2, lines 55-67 through column 3, lines 1-6 detail the first and second reset signals. Rejection maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-16 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent 6,877,112, Iino (hereinafter Iino).

6. Regarding claim 1 (and 9), Iino discloses:

A semiconductor integrated circuit device for emulating operation of a one-chip microcomputer having a CPU and a peripheral circuit that is controlled by the CPU (see Figure 4, "Emulator"), the device comprising:

a vector address switching circuit configured for outputting a vector address corresponding to a reset vector address supplied from the CPU when receiving a first reset signal, and for outputting a prescribed vector address instead of the vector address corresponding to the reset vector address supplied from the CPU when receiving a second reset signal (see column 2, lines 55-67,

column 3, lines 1-6; "first reset signal", "second reset signal"; see column 11, lines 43-47; it is well known in the art that reset signals output corresponding addresses to change programs); and

an interface circuit configured for performing input and output of information relating to emulation between the CPU and an external circuit (see column 2, lines 26-27, "the DSU has an interface to the emulator **401**),

wherein the CPU is configured to execute different programs depending on the vector address and the prescribed vector address output from the vector address switching circuit (see column 11, lines 43-47; "...executes processing from a reset vector which is a start address of a program to be loaded immediately after reset"; it is well known in the art that reset signals output addresses to change programs), and

wherein the CPU is constructed to be reset by the first and second reset signals and the interface circuit is constructed to be reset by the second reset signal but not by the first reset signal (see Figure 4: **13**, **21**; this is the definition of reset signals).

7. Regarding claim 2 (and 10), Iino discloses:

The semiconductor integrated circuit device according to claim 1, wherein:

the peripheral circuit includes a functional circuit for realizing a primary function of the peripheral circuit (column 1, lines 21-27, 'DSU'), a stop control circuit for stopping, in response to reception, by the CPU, of a break request that has occurred during execution of an instruction by the CPU (column 1, lines 28-40, "break command"), progress of an operation of the functional circuit until completion of processing that is performed in response to the break request (this is inherent in a break command), and a setting information storage circuit for storing

setting information indicating whether to enable or disable an operation stop function of the stop control circuit (see column 1, lines 28-39, "break command for generating a break-interrupt for load/store"); and

the functional circuit of the peripheral circuit is constructed to be reset by the first and second reset signals, and the stop control circuit and the setting information storage circuit are constructed to be reset by the second reset signal but not by the first reset signal (see column 2, lines 55-67, column 3, lines 1-6; this is the definition of reset signals).

8. Regarding claim 3 (and 11), Iino discloses:

The semiconductor integrated circuit device according to claim 1, further comprising:

an emulation memory for storing a user program that is executed by the CPU in response to the first reset signal (see column 2, lines 10-20); and

a monitor program memory for storing a monitor program that is executed by the CPU in response to the second reset signal (see column 1, lines 21-27).

9. Regarding claim 4 (and 12), Iino discloses:

The semiconductor integrated circuit device according to claim 1, wherein:

the CPU is operable in an normal operation mode and a low power consumption operation mode that is lower in power consumption than the normal operation mode (see column 1, lines 40-45); and

a break request control circuit is provided for causing a transition of the CPU to a break state after input of a wake-up signal for returning the CPU from the low power consumption

operation mode to the normal operation mode when a break request signal is input externally in a period when the CPU is in the low power consumption operation mode (see column 1, lines 28-39).

10. Regarding claim 5 (and 13), Iino discloses:

The semiconductor integrated circuit device according to claim 4, wherein the break request control circuit is constructed to immediately output a break request signal to the CPU if the break request signal is input in a period when the CPU is in the normal operation mode, and outputs a break request signals to the CPU upon input of the wake-up signal if the break request signal is input in a period when the CPU is in the low power consumption operation mode (see column 1, lines 28-45).

11. Regarding claim 6 (and 14), Iino discloses:

The semiconductor integrated circuit device according to claim 4, further comprising;

a break request control register that is reset by the second reset signal (see column 2, lines 55-63),

wherein the break request control circuit is constructed to cause a transition of the CPU to the break state immediately or after input of the wake-up signal when the break request signal is input externally in a period when the CPU is in the low power consumption operation mode depending on a value of the break request control register (see column 1, lines 28-39).

12. Regarding claim 7 (and 15), Iino discloses:

The semiconductor integrated circuit device according to claim 4, further comprising:

a wake-up signal generation circuit for generating a wake-up signal when a prescribed set time has elapsed from a transition of the CPU from the normal operation mode to the low power consumption operation mode (see column 1, lines 40-45).

13. Regarding claim 8 (and 16), Iino discloses:

The semiconductor integrated circuit device according to claim 7, wherein the wake-up signal generation circuit includes:

a counter for performing a counting operation in a period when the CPU is in the low power consumption operation mode (see column 9, line 61);

a storage circuit for storing a set count corresponding to the set time (see column 2, line 18); and a comparator circuit for comparing a value of the counter with the set count of the storage circuit, and for outputting the wake-up signal when the value of the counter has reached the set count (see column 10, lines 3-14).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nithya Janakiraman whose telephone number is 571-270-1003. The examiner can normally be reached on Monday-Thursday, 8:00am-5:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on (571)272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nithya Janakiraman
Art Unit 2123
December 17, 2007

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